Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **B1**
3. **CLR1**
4. **N. Q1**
5. **Q2**
6. **CEXT2**
7. **REXT2 CEXT**
8. **GND**
9. **A2**
10. **B2**
11. **CLR2**
12. **N. Q2**
13. **Q1**
14. **CEXT1**
15. **REXT1 CEXT**
16. **VCC**

**.071”**

**3**

**4**

**5**

**6**

**7**

**2 1 16 15**

**14**

**13**

**12**

**11**

**10**

**8 9**

**.114”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref: C18A**

**APPROVED BY: DK DIE SIZE .071” X .114” DATE: 11/15/21**

**MFG: NATIONAL THICKNESS .021” P/N: 54HC221**

**DG 10.1.2**

#### Rev B, 7/1